Exhibit

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Attorneys for Defendant
Lexar Media, Inc.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

SANDISK CORPORATION,

Plaintiff,

v.

LEXAR MEDIA, INC.,

Defendant.

AND RELATED COUNTERCLAIMS

Case No. C98-01115 CRB

SUPPLEMENTAL DECLARATION OF SEAN P. DEBRUINE IN SUPPORT OF MOTION FOR PARTIAL SUMMARY JUDGMENT OF INVALIDITY

Date: March 10, 2000
Time: 10:00am
Dept: 8
Judge: Hon. Charles H. Breyer

I, Sean P. DeBruine, declare as follows

1. I am an attorney with the law firm of Fenwick & West, LLP, counsel to defendant Lexar Media in this matter. I have personal knowledge of the following facts, and if called to testify I could and would testify competently to the matters set forth herein.

2. Attached hereto as Exhibit A is a true and correct copy of U.S. Patent 2,398,248 to Hsia, et al., along with the certificate of correction therefore issued by the U.S. Patent and Trademark Office.

3. Attached hereto as Exhibit B is a true and correct copy of the pertinent pages of the transcript of the deposition of Dr. Yukun Hsia taken by plaintiff SanDisk Corporation

("SanDisk") in this matter.

4. Attached hereto as Exhibit C are true and correct copies of the pertinent pages from the transcript of Dr. W. Milton Gosney taken by SanDisk in this matter.

5. Attached hereto as Exhibit D is a true and correct copy of the 1979 article entitled "Adaptive Wafer Scale Integration," by Dr. Hsia, *et al.* That paper is expressly incorporated by reference into Dr. Hsia's lecture notes. *See* Hsia Decl., Ex. G at LEX08553.

6. Attached hereto as Exhibit E is a true and correct copy of a report entitled "Adaptive Wafer Integration Technology Development, Volume III: Mass Memory System Description, Part I" dated May 23, 1979 by Dr. Hsia, which was marked as Exhibit 145 at Dr. Hsia's deposition. Page 3-52 (LEX15489) confirms that Dr. Hsia had conceived of partitioning each non-volatile memory sector into user data and overhead portions by 1979. In particular, that report discloses that "The eight additional [ECC] bits generated in this shift register are then appended onto the 64 data bits to form the 72-bit code word" stored in the nonvolatile memory sector.

7. Attached hereto as Exhibit F is a true and correct copy of the April, 1990 article by Iwata, *et al.*, entitled "A High-Density NAND EEPROM with Block-Page Programming for Microcomputer Applications." Figure 5 of that article shows that the 4mb NAND EEPROM chip consists of 4 1mb arrays.

I swear under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Executed this 25th day of February, 2000, at Palo Alto, California.

Sean P. DeBruine